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IMPLEMENTATION OF LOSSLESS ECG COMPRESSION ALGORITHM USING MODIFIED GOLOMB-RICE CODING FOR LOW POWER DEVICES

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Abstract

This paper presents a VLSI implementation of an efficient lossless compression scheme for electrocardiogram (ECG) data encoding to save storage space and reduce transmission time. This paper presents a novel hardware-oriented ECG compression algorithm and its very large-scale integration (VLSI) implementation for wireless sensor networks. The proposed novel ECG compression algorithm consists of a fuzzy decision, block partition, digital halftoning, and block truncation coding (BTC) techniques. A novel variable-size block partition technique was used in the proposed algorithm to improve ECG quality and compression performance. In addition, eight different types of blocks were encoded by Huffman coding according to probability to increase the compression ratio further. In order to achieve the low-cost and low-power characteristics, a novel iteration-based BTC training module was created to get representative levels and meet the requirement of wireless sensor networks. A prediction and modified Golomb-Rice coding modules were designed to encode the information of representative levels to achieve higher compression performance. The simulation results show that the proposed method resulted in superior performance as compared to the conventional approaches.

Index Terms— ECG Compression, Golomb Rice Coding, VLSI, Low Power Design, Adaptive Linear Prediction

I. INTRODUCTION

In recent years, cardiovascular disease (CVD) has been the major cause of death worldwide and is reported as roughly 31% of all global deaths [1]. To diagnose this disease and many others, the electrocardiogram (ECG) signal is used. ECG signal is a biomedical signal containing useful information about the heart condition and it is the most common

screening tool for cardiac disease diagnosis. In a 24-hour ECG signal monitoring system, the monitoring system will be producing a huge amount of data. To understand the amount of data generated during ECG monitoring process, following two different frequencies can be taken as examples. Normally at the sampling frequency of 125 Hz, 7.5 KB of ECG data is generated for the duration of 1 minute per sensor. If the sampling rate is 500 HZ then it will generate 45 KB of data per minute for one sensor [2]. So, to store this huge data, a solution is required to reduce the data of ECG signal.

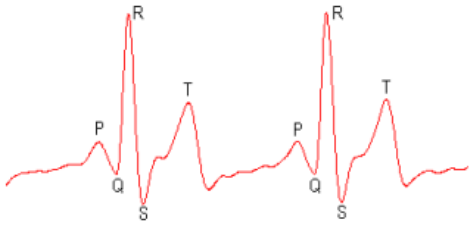

Figure 1: A typical ECG signal[14].

Recently, there has been an increase in the usage of wearable devices in health monitoring. These devices can perform many tasks, such as heart rate monitoring, walking or running steps counting, etc. Battery life is one of the important factors while designing different sensors or chip modules which lead to the need for developing low power hardware modules to be used in such devices. Many types of research on VLSI implementation of lossless ECG compression has been carried out in the past. Chen et al. [3] has presented a mixed signal VLSI design of ECG compression which includes a smart analog-to-digital converter (ADC) and lossless ECG compression is performed on the basis of trend forecasting and entropy coding. Although this design is intended for low power applications yet its power consumption is quite high which makes such design unsuitable for current low power devices. Another VLSI implementation of ECG compression has been proposed by Zou et al [4], which uses wavelet transform and Run-Length Encoding (RLE) but the working frequency of the design is quite high which makes it unsuitable to be used in real-time ECG data compression. The sampling frequency of ECG devices is in range of a few hundred hertz to one-kilo hertz [5], [6]. So, the design proposed by [4] is useful in the cases where ECG data has been already recorded in some storage and then compression is performed.

Yazicioglu et al. [7] has presented an ASIC for compression of ECG signals using ADC yet its power consumption is 30 µW. In this paper, VLSI implementation of the lossless ECG compression algorithm has been proposed developed on the work of Han and Guo [8] which introduces an ECG compression algorithm comprising of an adaptive linear

prediction technique as the prediction part and Golomb Rice code as entropy coding part. Adaptive linear prediction is based on previous samples to reduce the redundancy of the original data and is able to improve predictive accuracy to enhance the compression rate.

For entropy coding part, a content-adaptive Golomb-rice code (GRC) with a window size has been proposed to compress ECG data. For VLSI implementation, low power and real-time data processing technique has been proposed. The main aim of this work is low power design while using the minimum number of gates. Thus, this technique can be implemented in real-time ECG recording devices to consume less power.

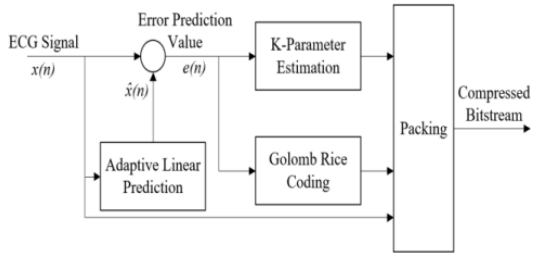

Fig. 2. Block diagram of the lossless ECG compression algorithm [8].

II. OVERALL SYSTEM & ALGORITHM

Generally, ECG data compression has two main processing parts i.e. error prediction and data coding as shown in Fig. 2. The prediction error value, e(n), can be calculated as (1)

$$e(n) = x(n) - \hat{x}(n) \quad (1)$$

where $\hat{x}(n)$ is the prediction value, and x(n) is the value of current sample data in ECG data at time n. This prediction error value is utilized in Golomb code.

A. Adaptive Linear Prediction

ECG signal contains numerous regions with sharp amplitude variations, such as QRS, P, and T wave regions, as shown in Fig. 1, which may result in a higher prediction error during prediction error estimation phase. In [8], an adaptive linear predictor technique is proposed to improve the prediction error by keeping its value minimum. Previous four samples are used to estimate the prediction value, which has been shown in fig. 3. The value of the four parameters i.e. 'D1_2', 'D1_3', 'D2_3', and 'D3_4' is calculated through the following equations;

$$D1\_2\,(n) = x\,(n\text{-}1) - x\,(n\text{-}2) \quad (2)$$

$$D1\_3\,(n) = x\,(n\text{-}1) - x\,(n\text{-}3) \quad (3)$$

$$D2\_3\,(n) = x\,(n\text{-}2) - x\,(n\text{-}3) \quad (4)$$

$$D3\_4\,(n) = x\,(n\text{-}3) - x\,(n\text{-}4) \quad (5)$$

Taking the characteristics of the ECG signal into consideration, the simple differential predictors with coefficients are used. Due to low complexity computation an good performance in estimating prediction value, the following three differential predictors have been selected in algorithm development as shown in (6), (7) and (8). A detailed discussion on the

derivation of the equations (2) to (8) can be found in [8].

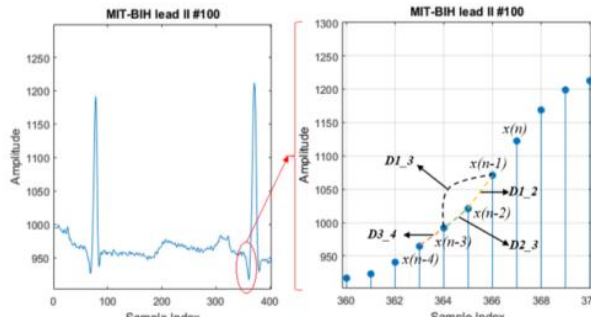

Figure 3: Relation between previous four samples.

$$P1: \hat{x}(n) = x(n-1) \quad (6)$$

$$P2: \hat{x}(n) = 2x(n-1) - x(n-2) \quad (7)$$

$$P3: \hat{x}(n) = 3x(n-1) - 3x(n-2) + x(n-3) \quad (8)$$

B. Lossless Data Compression Technique

Entropy coding is the part of coding technique in data compression, in which frequently occurring patterns or values are presented with few binary bits and rarely occurring ones are presented with many binary bits. Built on the work of [9], the reference software implementation uses a low-complexity entropy encoder i.e. Golomb–Rice code [8].

C. Content-Adaptive Golomb-Rice code

Golomb coding is a data compression scheme based upon entropy encoding and is optimal for alphabets with a geometric distribution. The Golomb-Rice code comprises two parts: quotient and remainder, which are represented by

$$\begin{cases} quotient: \left\lfloor \frac{M[n]}{2^k} \right\rfloor; & encode\ with\ unary\ code \\ remainder: M[n] \bmod 2^k; & encode\ with\ binary\ code \end{cases} \quad (9)$$

where k represents the number of bits for the remainder, and M[n] is a positive integer. M[n] is achieved by transformation of a prediction error, which may be a negative value, into a positive number. This function can be described by

$$M[n] = \begin{cases} 2e, & e \geq 0 \\ 2|e| - 1, & e < 0 \end{cases} \quad (10)$$

where e is the prediction error value. In algorithm development, a window is used to calculate the distribution of prediction errors [8]. The distribution of prediction error of each window is applied to determinate the k parameter. The size of the window is determined using the QRS segment in the ECG signal.

D. Data Packing Format

In the decoding process, to reconstruct the original signal, the encoded output stream contains the first sample of ECG data of 11-bits and the k parameter with 3-bits for each window and prediction error which is encoded by Golomb-Rice code. The output bit stream is illustrated in Fig. 5.

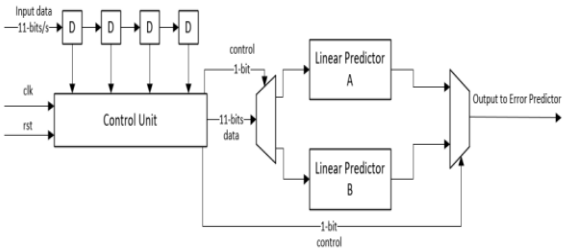

Fig. 4. Hardware architecture for data processing for ALP.

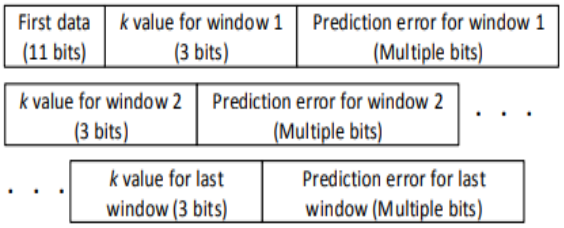

Fig. 5. Encoded bitstream format.

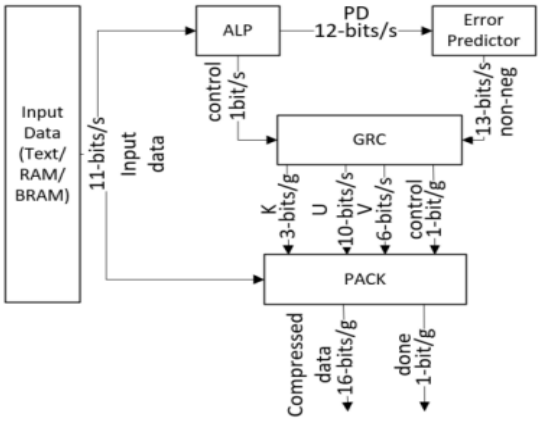

Fig. 6. Block level diagram for hardware implementation.

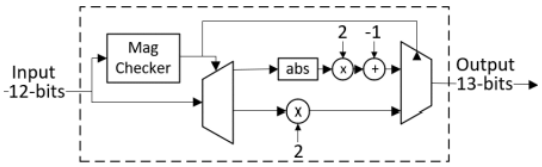

Fig. 7. The hardware architecture for error predictor.

III. HARDWARE ARCHITECTURE

For the hardware implementation, Fig. 6 shows a block level diagram. Input data's source can be RAM, BRAM or text file and the input data has 11 bits per sample which are processed in Adaptive Linear Prediction (ALP) module in the first phase. After performing the error prediction, Golomb Rice coding (GRC) is performed on the processed data. In the last stage, the packing is performed and data is sent as output where data becomes valid in the form of a group. The detailed implementation of each module will be discussed in the following section.

A. Adaptive Linear Prediction & Error Prediction

For ALP module, 11-bit input is being processed at every clock cycle. For the first four inputs, linear prediction is performed differently as compared to other inputs as discussed in the proposed original algorithm [8]. This leads to the designing of two different linear predictors. In Fig. 4, a control unit is controlling the input data by generating control signals for the selection of linear prediction unit as well as sending data from linear prediction units to error predictor. For error predictor, simple arithmetic is present to check whether the number is positive or negative. In error predictor, input data is coming from linear prediction module. Figure 7 represents the hardware architecture for error prediction module. The sign bit, which is added in ALP processing, is being evaluated to check whether the number is positive or negative.

B. Golomb Rice Coding

Golomb rice coding is the most complex and computation intense part in the whole compression algorithm. And due to continuous data processing, the hardware

design is designed to keep minimum delay for data processing in Golomb Rice coding. Moreover, area saving techniques were implemented so that the chip area does not get big. Figure 8 shows the hardware architecture design for Golomb Rice coding module. Input data is post-processed data of the error predictor module. Data is processed for one complete window so there is a 40x13-bits register to save one window's values. When new window's values are arriving then previous window's values are processed to find the value of U and V, where U and V represent quotient and remainder respectively. So, in general, this module's architecture can be divided into two parts; data controlling part and computation part as shown in Fig. 8. In the computation part, operations have been divided into different clock cycles to reduce the processing delay. Instead of using the built-in operators of division or power, bit shifting has been used to perform the multiplication, power, mod and division operations. By using this bit tweaking, the design is able to benefit from the reduction of a number of gates and power consumption. For example, division and multiplication of a number by two have been performed by shifting the value to right and left by 1 bit respectively.

Moreover, division is performed after the summation of the values of one window, the range of values will be between 1 to 127. So, the log values of these values have been stored in a log table, which is accessed whenever a log operation is required in the design. A single counter is being used to control data reading and saving to reduce resources usage. Moreover, sharing of the single counter for both controllers leads to less activity as compared to using two counters which results in saving switching power.

C. Packaging Packaging

module includes two controllers which are responsible for data saving in a temporary 26-bits register as well as sending 16-bits of output data when 16 or more than 16 bits have been stored in the temporary register. The hardware architecture for packaging module is shown in Fig. 9.

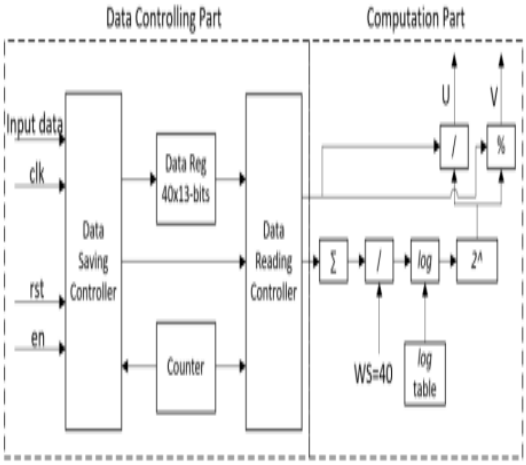

Fig. 8. Hardware architecture for Golomb Rice coding.

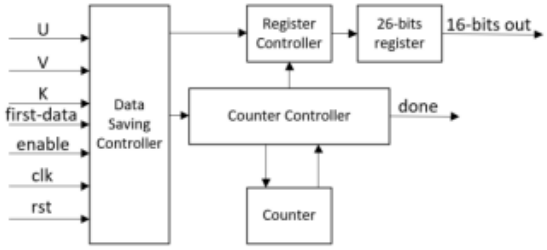

Fig. 9. The hardware architecture for packaging module.

D. Modified GR Decoding

Fig. 10 shows the flowchart of the decoding process of the modified GR. First, the number of bit "0" is counted before segmentation, the first bit "1", shows up. Second, the next 3 bits is identified as a sign bit and 2 bits of the remainder. Third, if absolute of prediction error is greater than or equal to 32, it won't take any advantage of entropy coding. Moreover, it takes more bits than the binary representation. This is the reason why the value greater than or equal to 32 was encoded with binary representation after an impossible circumstance code (negative zero encoded with signed GR coding) which is to tell decoder the following 8 bits are binary representation. Finally, if value is encoded in binary representation, it could be outputted directly. Otherwise, the sign information will be added to the final decoded value according to the decoded value of the sign bit.

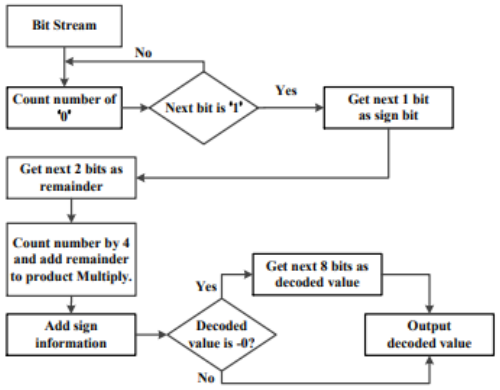

Figure 10: Flowchart of the decoding process for the signed GR coding.

IV. SIMULATION RESULTS

In this study, we used Xilinx ISE to verify the feasibility of the proposed lossless image compression algorithm. First, we used the system level design simulation results to make the goal of the complexity and compression ratios. After determining the algorithm, Verilog codes were written according to the developed algorithm. Next, the Verilog codes were processed by logic synthesis with a ISE Design Compiler tool.

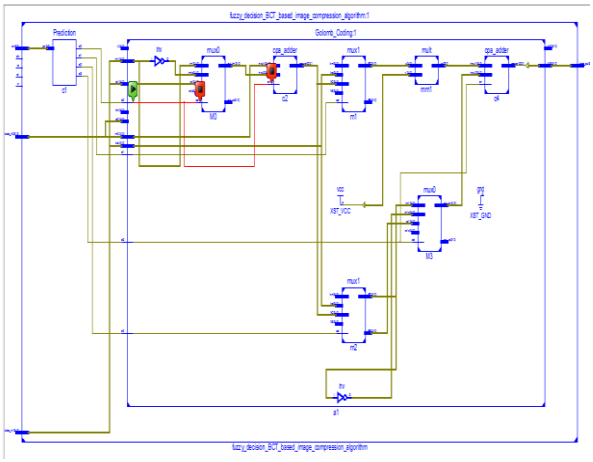

Figure 11: 1 RTL Schematic

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	1752	204000	0%
Number of fully used LUT-FF pairs	0	1752	0%
Number of bonded IOBs	100	600	16%

Figure 12: DESIGN SUMMARY

```
LUT3:I0->O            1    0.043   0.289  a1/mm1/Madd_n06166 (a1/mm1/Madd_n06166)
LUT4:I3->O            1    0.043   0.000  a1/mm1/Madd_n0616_lut<0>25 (a1/mm1/Madd_n0616_lut<0>2
MUXCY:S->O            1    0.230   0.000  a1/mm1/Madd_n0616_cy<0>_24 (a1/mm1/Madd_n0616_cy<0>2
XORCY:CI->O           2    0.251   0.432  a1/mm1/Madd_n0616_xor<0>_25 (a1/mm1/n0616<26>)
LUT3:I0->O            1    0.043   0.289  a1/mm1/Madd_n06224 (a1/mm1/Madd_n06224)
LUT4:I3->O            1    0.043   0.000  a1/mm1/Madd_n0622_lut<0>27 (a1/mm1/Madd_n0622_lut<0>2
MUXCY:S->O            1    0.230   0.000  a1/mm1/Madd_n0622_cy<0>_26 (a1/mm1/Madd_n0622_cy<0>2
XORCY:CI->O           2    0.251   0.432  a1/mm1/Madd_n0622_xor<0>_27 (a1/mm1/n0622<28>)
LUT3:I0->O            1    0.043   0.289  a1/mm1/Madd_n06282 (a1/mm1/Madd_n06282)
LUT4:I3->O            1    0.043   0.000  a1/mm1/Madd_n0628_lut<0>29 (a1/mm1/Madd_n0628_lut<0>2
MUXCY:S->O            1    0.230   0.000  a1/mm1/Madd_n0628_cy<0>_28 (a1/mm1/Madd_n0628_cy<0>2
XORCY:CI->O           1    0.251   0.289  a1/mm1/Madd_n0628_xor<0>_29 (a1/mm1/Madd_prod_lut<30>
LUT1:I0->O            1    0.043   0.000  a1/mm1/Madd_prod_cy<30>_rt (a1/mm1/Madd_prod_cy<30>_r
MUXCY:S->O            0    0.230   0.000  a1/mm1/Madd_prod_cy<30> (a1/mm1/Madd_prod_cy<30>)
XORCY:CI->O           1    0.251   0.542  a1/mm1/Madd_prod_xor<31> (a1/PCA<31>)
LUT5:I0->O            1    0.043   0.279  a1/c4/generate_N_bit_Adder[31].f/Mxor_s_xo<0>1 (data_
OBUF:I->O                 0.000          data_out_31_OBUF (data_out<31>)
----------------------------------------
Total                      14.327ns (4.923ns logic, 9.404ns route)
                                    (34.4% logic, 65.6% route)
```

Figure 13: TIME SUMMARY

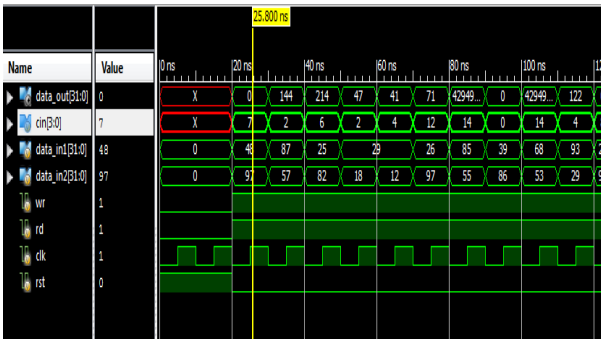

Figure 14: Simulation outcome

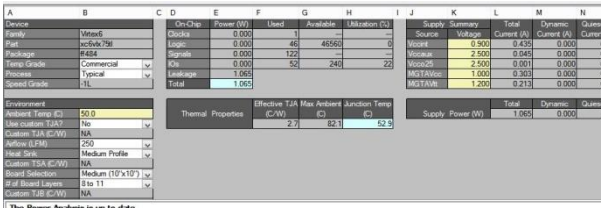

Figure 15: Power summary

Conclusion:

An efficient scheme for Compression electro cardiac signal data has been implemented with reduced number of computations using DCA scheme. Proposed scheme performed excellent simulation results over conventional Compression schemes in terms of storage in number of bytes. An efficient method for arrhythmia detection has been developed based on heart rate. EMD based method for Compression of ECG signal is proposed in which Automatic detection of noisy IMFs is done using Spectral Flatness measure. After Enhancement, R Peak detection, the most relevant feature of an ECG waveform is done using Threshold methodology. Once R peak is detected, RR interval is calculated to estimate the heart rate for arrhythmia detection.

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